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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/715,410 | 11/19/2003 | David Walter Flynn | 550-490 | 5318 |

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| EXAMINER | |
|---|---|
| CRIBBS, MALCOLM D | |
| **ART UNIT** | **PAPER NUMBER** |
| 2115 | |

DATE MAILED: 04/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/715,410 | FLYNN, DAVID WALTER | |
| | Examiner | Art Unit | |
| | Malcolm D. Cribbs | 2115 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *19 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/19/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

***1. Claims 1-20 are presented for examination.***

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horden et al [US Patent No. 5,812,860; cited by applicant per IDS received on 11/19/2003] in view of Shaffer et al [US Patent No. 6,298,448].

4. As per claim 1, Horden et al teach the invention comprising:

a processor operable to generate a performance control signal indicative of a desired data processing performance level [Col 3 lines 9-10]; and

one or more further circuits responsive to the performance control signal [Col 3 lines 24-28].

5. Horden et al do not teach a method of the circuits generating a signal indicative of their current operation. Specifically, Horden et al teach controlling the performance of a system using a control signal indicating to the clock generator and the voltage

regulator to select a different level of performance, which consumes valuable time while switching between high and low power. However, Horden et al fail to detail a method of the other circuits operable to output their current operation. A routineer in the art would have been motivated to look for a teaching for the possible method of reducing the time required for switching performance levels of a processor.

6. Shaffer et al teach another method of controlling the performance of a processor with other circuits responsive to a performance control signal sent from the processor. Shaffer et al teach other circuits, for example the clock module, operable to inform the processor of its current output frequency, current operation [Col 3 lines 12-22]. In summary, Shaffer et al teach a processor always knowing what the other circuits current operations with an automatic change instead of wasting time in a higher power level.

7. It would have been obvious to one of ordinary skill in the art to combine the teachings of Horden et al and Shaffer et al, which are analogous art, because they both teach a method of controlling the performance of a processor for power consumption purposes. Shaffer et al cover the deficiency of Horden et al by teaching the detail of the other circuits operable to output their current operation.

8. As per claim 2, Horden et al teach the invention of the further circuits including a voltage controller to generate a power signal for the processor at a plurality if different voltage levels [Col 4 lines 12-16].

9. As per claim 3, Shaffer et al teach the invention of the further circuits including a clock generator [clock module] with selectable clock frequencies [Col 3 lines 12-22].

10. As per claims 4, 6, 9, are obvious to one of ordinary skill in the processor performance control art because in order to switch performance levels the processor must increase or decrease its clock speed and power thereto. Therefore, the clock and voltage regulator would increase or decrease these circuits accordingly.

11. As per claim 5, Shaffer et al teach the invention of a PPL circuit [Fig 1, 20, 49, 51; where the feedback of the clock module is used to output the proper operating frequency].

12. As per claim 7, Horden et al teach the invention of intermediate levels [Col 4 lines 12-14].

13. As per claim 8, Shaffer et al teach the invention of a clock generator with selectable clock frequencies [Col 2 lines 62-67].

14. As per claim 10 Horden et al teach the invention of supporting a maximum level independent of the performance control signal [Col 4 lines 42-54].

15. As per claims 11-20, it is directed to the method of steps to implement the system as set forth in claims 1-10. Therefore, it is rejected for the same basis as set forth hereinabove.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Malcolm D. Cribbs whose telephone number is 571-272-5689. The examiner can normally be reached on M-F 8AM-430PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Malcolm D Cribbs
Examiner
Art Unit 2115

April 18, 2006

CHUN CAO
PRIMARY EXAMINER